PXIe-5110 Specifications

Contents

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These specifications apply to the PXIe-5110 with 64 MB and 512 MB of memory.

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. Warranted specifications account for measurement uncertainties, temperature drift, and aging. Warranted specifications are ensured by design or verified during production and calibration.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- **Measured** specifications describe the measured performance of a representative model.

Specifications are **Nominal** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All vertical ranges, bandwidths, and bandwidth limiting filters
- Sample rate set to 0.5 GS/s or 1 GS/s
- Onboard sample clock locked to PXI_Clk100 reference clock
- 15-minute warm-up time at ambient temperature
- Chassis configured:[1]

- PXI Express chassis fan speed set to HIGH
- Foam fan filters removed if present
- Empty slots contain PXI chassis slot blockers and filler panels

Warranted specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature range of 0 °C to 55 °C
- Altitude ≤2,000 m
- Calibration cycle maintained
- Self-calibration run after:
  - Warm-up time has elapsed
  - Module has been power cycled
  - PC or controller has been restarted or wakes from sleep or hibernation modes
- External calibration performed at 23 °C ±3 °C

Typical specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature range of 0 °C to 55 °C
- Altitude ≤2,000 m

Vertical

Analog Input

Number of channels	Two (simultaneously sampled)
Input type	Referenced single-ended
Connectors	BNC, ground referenced

Impedance and Coupling

Input impedance	50 Ω ±1.5%, typical 1 MΩ ±1.0%, typical
Input capacitance (1 MΩ)	16 pF
Input coupling	AC DC

Voltage Levels

Table 1. Full-Scale (FS) Input Range and Vertical Offset Range

Input Range (V_{pk-pk})	Vertical Offset Range	
	50 Ω	1 MΩ
0.04 V	±5 V	
0.1 V	±5 V	
0.2 V	±5 V	
0.4 V	±5 V	
1 V	±5 V	±20 V
2 V	±5 V	±20 V
4 V	±5 V	±20 V
10 V	±2 V	±100 V
20 V	—	±100 V
40 V	—	±100 V

Maximum input overload

50 Ω	|Peaks| ≤7 V
1 MΩ[2]	|Peaks| ≤250 V DC

Notice Signals exceeding the maximum input overload may cause damage to the device.

Accuracy

Resolution	8 bits
DC accuracy[3]	
50 Ω	
Input range: 0.04 V	±[(2% × |**Reading** - **Vertical Offset**|) + (0.4% × |**Vertical Offset**|) + (1% of FS)+ 0.2 mV], typical
Input range: 0.1 V to 4 V	±[(2% × |**Reading** - **Vertical Offset**|) + (0.4% × |**Vertical Offset**|) + (1% of FS)+ 0.2 mV], warranted
Input range: 10 V	±[(2% × |**Reading** - **Vertical Offset**|)+ (1.1% × |**Vertical Offset**|) + (1% of FS)+ 0.2 mV], warranted
1 MΩ	
Input range: 0.04 V	±[(2% × |**Reading** - **Vertical Offset**|) + (0.4% × |**Vertical Offset**|) + (1% of FS)+ 0.2 mV], typical
Input range: 0.1 V to 20 V	±[(2% × |**Reading** - **Vertical Offset**|) + (0.4% × |**Vertical Offset**|) + (1% of FS)+ 0.2 mV], warranted
Input range: 40 V	±[(2% × |**Reading** - **Vertical Offset**|)+ (1.1% × |**Vertical Offset**|) + (1% of FS)+ 0.2 mV], warranted
DC drift[4]	±[(0.036% × |**Reading** - **Vertical Offset**|)+ (0.004% × |**Vertical Offset**|) + (0.012% of FS)] per °C
AC amplitude accuracy[3]	±0.25 dB at 50 kHz

AC amplitude drift[4]	±0.0046 dB per °C at 50 kHz

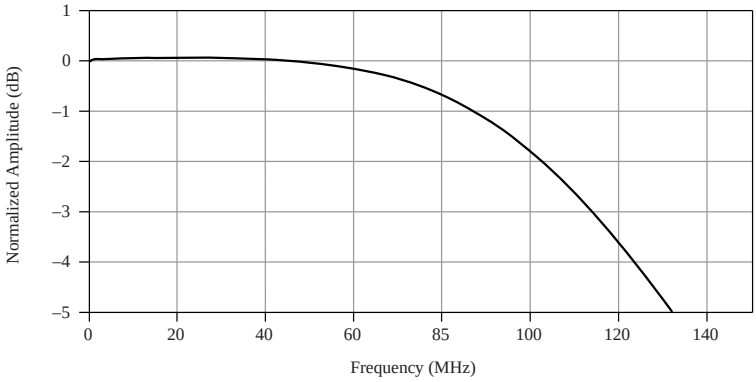
Crosstalk

Crosstalk[5]	<-65 dB at input frequencies ≤100 MHz

Bandwidth and Transient Response

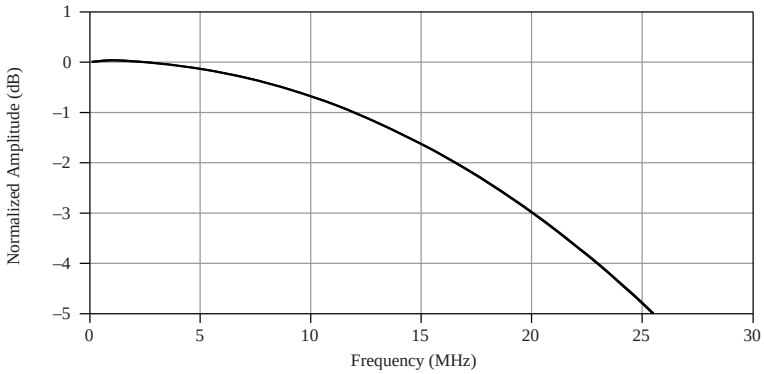
Bandwidth (-3 dB)[6]	
50 Ω	100 MHz, warranted
1 MΩ	100 MHz, typical

Figure 1. 50 Ω Full Bandwidth Frequency Response, 1 GS/s, 1 $V_{pk\text{-}pk}$, Measured[6]



Bandwidth-limiting filter	20 MHz noise filter

Figure 2. 50 Ω 20 MHz Filter Frequency Response, 1 GS/s, 1 $V_{pk\text{-}pk}$, Measured[6]



AC-coupling cutoff (-3 dB)	10 Hz

Figure 3. Step Response, 50 Ω, 1 V_{pk-pk}, 500 ps Rising Edge, Measured

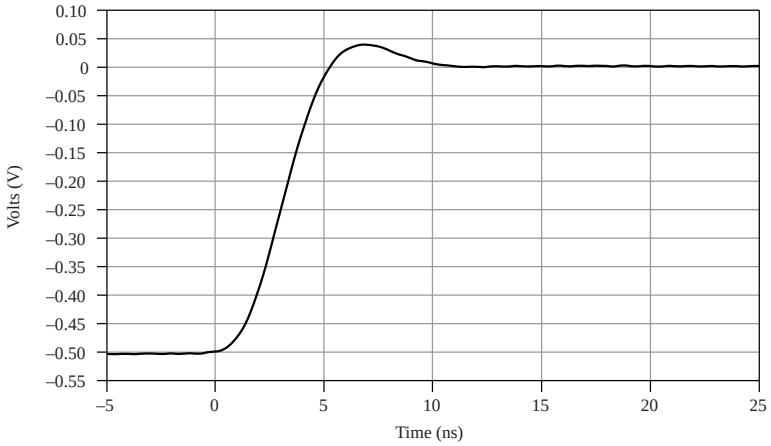
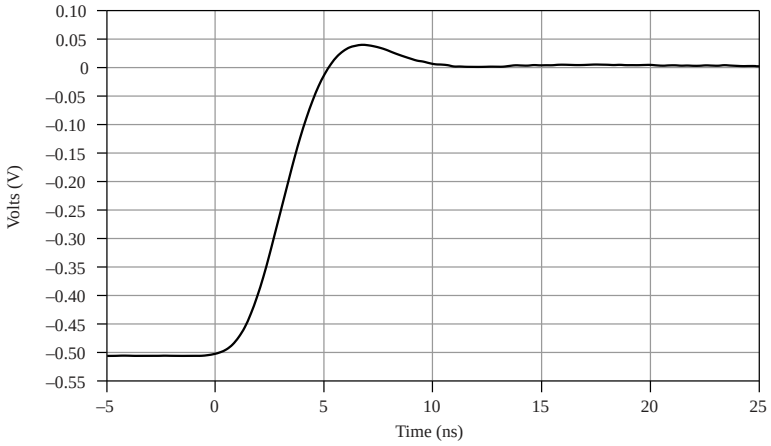


Figure 4. Step Response, 1 MΩ, 1 V_{pk-pk}, 500 ps Rising Edge, Measured



Spectral Characteristics[7]

Spurious-free dynamic range (SFDR)[8]	-50 dBc

Table 2. Effective Number of Bits (ENOB)[9]

Input Range (V_{pk-pk})	Filters	
	20 MHz filter enabled	Full bandwidth (Input Frequency <50 MHz)
0.1 V to 4 V	7.2	6.9
0.04 V	6.8	6.6

Total harmonic distortion (THD)[8]	-50 dBc

Noise

RMS noise[10]	0.3% of FS

Horizontal

Sample Clock

Source	Onboard clock (internal oscillator)
Sample rate range, real time[11]	7.63 kS/s to 500 MS/s
Sample rate, time-interleaved sampling (TIS) mode[12]	1 GS/s
Timebase frequency	500 MHz
Timebase accuracy[13]	±50 ppm
Sample clock jitter[14]	2 ps RMS

Phase-Locked Loop (PLL) Reference Clock

Sources	
Internal	Onboard clock (internal oscillator)
External	PXI_Clk100 (backplane connector)
Duty cycle tolerance	45% to 55%, typical

Triggers

Supported triggers	Reference (Stop) Trigger Reference (Arm) Trigger

	Start Trigger (Acquisition Arm) Advance Trigger
Trigger types	Edge Glitch Hysteresis Runt Width Window Digital Immediate Software
Trigger sources	CH 0 CH 1 PFI <0..3> PXI_Trig <0..7>

Minimum dead time

Interpolator enabled	600 ns
Interpolator disabled	400 ns

Trigger delay	0 to 2.25 × 10^{15} ns [(2^{51} - 1) * **Sample Clock Period**]
Holdoff	Dead time to 1.84 × 10^{19} ns [(2^{64} - 1) * **Sample Clock Period**]

Analog Trigger

Sources	CH 0 CH 1

Table 3. Analog Trigger Time Resolution

Interpolator Status	Time Resolution	
	TIS Enabled	TIS Disabled
Enabled	0.977 ps	1.95 ps
Disabled	1 ns	2 ns

Trigger filters	
Low frequency (LF) reject	100 kHz
High frequency (HF) reject	100 kHz
Minimum threshold duration[15]	**Sample clock period**

Digital Trigger

Sources	PFI <0..3> (front panel HD-BNC connectors) PXI_Trig <0..7> (backplane connector)

Time resolution	
PFI	2 ns

PXI_Trig	8 ns

Programmable Function Interface (PFI)

Connectors	PFI <0..3> (front panel HD-BNC connectors)
Direction	Bidirectional per channel

As an input (trigger)

Destinations	Start Trigger (Acquisition Arm) Reference (Stop) Trigger Reference (Arm) Trigger Advance Trigger
Input impedance	49.9 kΩ
V_{IH}	2 V, typical
V_{IL}	0.8 V, typical
Recommended input range	0 V to 3.3 V
Maximum input overload	+5 V tolerant
Minimum pulse width	10 ns

As an output (event)

Sources	Ready for Start

	Start Trigger (Acquisiton Arm) Ready for Reference Reference (Stop) Trigger End of Record Ready for Advance Advance Trigger Done (End of Acquisition)
Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum current drive	12 mA
Maximum frequency	50 MHz
Minimum pulse width	10 ns

Probe Compensation

Connectors	Probe compensation terminal Ground terminal
Output voltage[16]	0 V to 5 V
Maximum overload voltage	25 V DC

CableSense

CableSense pulse voltage[17]	0.4 V
CableSense pulse rise time[18]	4 ns

Driver support for CableSense on the PXIe-5110 was first available in NI-SCOPE18.7.

Related information

- For more information about CableSense technology, refer to ni.com/cablesense.

Waveform Memory

Available onboard memory sizes[19]	64 MB 512 MB
Minimum record length	1 sample
Number of samples Pretrigger — 0 up to (**Record Length** - 1) Posttrigger — 0 up to **Record Length**	
Maximum number of records in onboard memory[20]	100,000

Table 4. Examples of Allocated Onboard Memory per Record, 512 MB Option

Channels	Bytes per Sample	Maximum Records per Channel	Record Length	Allocated Onboard Memory per Record
1	1	100,000	1	192
1	1	100,000	1,000	1,200

Channels	Bytes per Sample	Maximum Records per Channel	Record Length	Allocated Onboard Memory per Record
1	1	52,924	10,000	10,176
1	1	1	536,870,785	536,870,976
2	1	100,000	1	192
2	1	100,000	1,000	2,208
2	1	26,672	10,000	20,160
2	1	1	268,435,393	536,870,976

Calibration

External Calibration

External calibration corrects the onboard references for gain and offset errors used in self-calibration and adjusts the compensation attenuator. All calibration constants are stored in nonvolatile memory.

Self-Calibration

Self-calibration is done on software command. The calibration corrects for gain, offset, interleaving spurs, and intermodule synchronization errors. Run self-calibration after the specified warm-up time has elapsed and any time the module is power cycled or the PC or controller is restarted or wakes from sleep or hibernation modes. Refer to the **NI High-Speed Digitizers Help** at ni.com/manuals for more information on when to self-calibrate the device.

Calibration Specifications

Interval for external calibration	2 years
Warm-up time[21]	15 minutes

Software

Driver Software

Driver support for this device was first available in NI-SCOPE18.6.

NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the PXIe-5110. NI-SCOPE provides application programming interfaces for many development environments.

Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can use InstrumentStudio to monitor, control, and record measurements from the PXIe-5110.

InstrumentStudio is an application that allows you to perform interactive measurements on several different NI device types in a single application.

Interactive control of the PXIe-5110 was first available via InstrumentStudio in NI-SCOPE18.6. InstrumentStudio is included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PXIe-5110. MAX is included on the driver media.

Synchronization

Channel-to-channel skew, between the channels of a PXIe-5110	
50 Ω	<100 ps
1 MΩ	<100 ps

Synchronization with the NI-TClk API [22]

NI-TClk is an API that enables system synchronization of supported PXI modules in one or more PXI chassis, which you can use with the PXIe-5110 and NI-SCOPE.

NI-TClk uses a shared Reference Clock and triggers to align the Sample Clocks of PXI modules and synchronize the distribution and reception of triggers. These signals are routed through the PXI chassis backplane without external cable connections between PXI modules in the same chassis.

Module-to-module skew, between PXIe-5110 modules using NI-TClk [23]	
NI-TClk synchronization without manual adjustment [24]	
Skew, peak-to-peak [25]	200 ps
Jitter, peak-to-peak [26]	120 ps
NI-TClk synchronization with manual adjustment [24]	
Skew, average [25]	10 ps
Jitter, peak-to-peak [26]	8 ps
Sample Clock delay/adjustment resolution	<1 ps

Power

Current draw	
+3.3 V DC	1.82 A
+12 V DC	0.83 A
Power draw	
+3.3 V DC	6 W
+12 V DC	10 W
Total	16 W
Total maximum power allowed	30 W

Physical

Dimensions	3U, one-slot, PXI Express/CompactPCI Express module 2.0 cm × 13.0 cm × 21.6 cm (0.8 in × 5.1 in × 8.5 in)
Weight	380 g (13.4 oz)

Bus Interface

Form factor	Gen 1 x4 module
Slot compatibility	PXI Express or hybrid

Environmental Characteristics

Temperature	
Operating	0 °C to 55 °C
Storage	-40 °C to 71 °C
Humidity	
Operating	10% to 90%, noncondensing
Storage	5% to 95%, noncondensing
Pollution Degree	2
Maximum altitude	4,600 m (at 25 °C ambient temperature)
Shock and Vibration	
Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

[1] For more information about cooling, refer to the **Maintain Forced-Air Cooling Note to Users** available at ni.com/manuals.

[2] Derate above 250 kHz at 20 dB/dec until 2.5 MHz, then derate at 5 dB/dec.

[3] Within ±5 °C of self-calibration temperature.

[4] Used to calculate errors when the onboard temperature changes more than ±5 °C from the self-calibration temperature.

[5] Measured on one channel with test signal applied to another channel and the same range setting on both channels.

[6] Normalized to 50 kHz.

[7] Excludes ADC interleaving spurs.

[8] Input frequencies <50 MHz, input range ≤4 V_{pk-pk}. -1 dBFS input signal. Includes second through fifth harmonics.

[9] Input frequencies <50 MHz. -1 dBFS input signal corrected to FS. 1 kHz resolution bandwidth.

[10] Applies to all filter settings and input modes. Verified using a 50 Ω terminator connected to input.

[11] Divide by **n** decimation from 500 MS/s. For more information on the sample clock and decimation, refer to the **NI High-Speed Digitizers Help**.

[12] Single channel only.

[13] Phase-locked to onboard clock. The default clock is PXI_Clk100. Refer to your chassis specifications for the timebase accuracy of PXI_Clk100.

[14] Integrated from 100 Hz to 10 MHz. Includes the effects of converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.

[15] Data must exceed each corresponding trigger threshold for at least this minimum duration to ensure analog triggering.

[16] 1 kHz, 50% duty cycle square wave.

[17] When measured with a high-impedance device.

[18] When sourcing into a 50 Ω cable or load.

[19] Onboard memory is shared among all enabled channels.

[20] For 512 MB option. You can exceed this value if you fetch records while acquiring data. For more information, refer to the Enable Records > Memory property in the **NI High-Speed Digitizers Help** at ni.com/manuals.

[21] Warm-up time begins after the chassis and either the controller or PC is powered and NI-SCOPE is loaded.

[22] NI-TClk installs with NI-SCOPE.

[23] Although you can use NI-TClk to synchronize non-identical modules, these specifications apply only to synchronizing identical modules. Specifications are valid under the following conditions:

- All modules installed in the same PXI Express chassis
- NI-TClk used to align the sample clocks of each module
- All parameters set to identical values for each module
- Self-calibration completed
- Ambient temperature within ±1 °C of self-calibration

For other configurations, including multi-chassis systems, contact NI Technical Support at ni.com/support.

[24] Manual adjustment is the process of minimizing synchronization jitter and skew by adjusting Trigger Clock (TClk) signals using the instrument driver.

[25] **Skew** is the misalignment between module timing across slots of a chassis and is caused by clock and analog path delay differences.

[26] **Jitter** is the variation in module alignment that can be expected with each call to NI-TClkSynchronize.